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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,134	02/20/2004	Gerd Frankowsky	INF 2233-US	5383

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ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/784,134	FRANKOWSKY, GERD	
	Examiner	Art Unit	
	Saqib J. Siddiqui	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-12,14-20 and 22-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-12,14-20 and 22-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's response was received and entered March 12, 2007.

- Claims 1, 4-12, 14-20 & 22-24 are pending.
- Claims 1, 7, 15, & 18 are amended.
- Claims 22-24 are new.

Response to Amendment

Applicant's arguments and amendments with respect to claims 1-24 filed March 12, 2007 have been fully considered but they are moot under new grounds of rejection. The Examiner would like to point out that this action is made final (See MPEP 706.07a).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1. 4-5, 7-10, 14-19 and 22-24 are rejected under 35 U.S.C. 102(b) as being fully anticipated by Beffa et al. US Pat no. 6,145,092.

As per claims 1, 7, 15 and 18:

Beffa et al. teaches a method, test device, test system and method for determining for determining a repair solution for a memory module in a test system, comprising: determining, for each memory area of the memory module a defect datum; generating defect addresses for all defective memory areas (column 5, lines 1-15);

storing the defect addresses in the test system (column 4, lines 30-60); and selecting one or more replacement redundant groups based on the defect addresses stored in the test system (column 5, lines 15-27), wherein each memory area is addressable via a word line group comprising one or more word lines or via a bit line group comprising one or more bit lines (column 5, lines 45-60) , and wherein the one or more replacement redundant groups are selected from a redundant word line group if the defective memory areas that are addressable by a common word line group exceeds a first maximum number of defective memory areas and from a redundant bit line group if the defective memory areas that are addressable by a common bit line group exceeds a second maximum number of defective memory areas (Figure 2 # 216 & # 218, claim 29).

As per claims 4, 8, 10 and 19:

Beffa et al. teach the method as rejected in claim 1 above, wherein the first maximum number corresponds to available redundant bit line groups and the second maximum number corresponds to available redundant word line groups (claims 14 and 15).

As per claims 5 and 9:

Beffa et al. teaches a method as rejected in claim 1 above, wherein defect addresses are stored in a memory unit which includes a first memory segment having a first number of defect address memory locations for storing defect addresses in a word line group and a second memory segment having a second number of defect address memory locations for storing defect addresses in a bit line group (Figure 2 # 206 & 208).

As per claims 14 and 16-17:

Beffa et al. teaches the test device as rejected in claim 7 above, further comprising a comparator circuit for comparing written data and read-out data to generate defect data (Figure 2 # 224).

As per claims 22-24:

Beffa et al. teaches a method, test device, test system and method for determining for determining a repair solution for a memory module in a test system as rejected above, wherein the one or more replacement redundant groups are selected for all remaining defective memory areas that were not replaced by one of the redundant word line group and the redundant bit line group (Figure 6b # 640).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 6, 11-12 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beffa et al. US Pat no. 6,145,092 and further in view of Bemis US Pat no. 4,692,894 A.

As per claims 6, 11-12 and 20:

Beffa et al. substantially teaches a method, test device, test system and method for determining for determining a repair solution for a memory module in a test system, comprising: determining, for each memory area of the memory module a defect datum; generating defect addresses for all defective memory areas (column 5, lines 1-15); storing the defect addresses in the test system (column 4, lines 30-60); and selecting one or more replacement redundant groups based on the defect addresses stored in the test system (column 5, lines 15-27), wherein each memory area is addressable via a word line group comprising one or more word lines or via a bit line group comprising one or more bit lines (column 5, lines 45-60) , and wherein the one or more replacement redundant groups are selected from a redundant word line group if the defective memory areas that are addressable by a common word line group exceeds a first maximum number of defective memory areas and from a redundant bit line group if the defective memory areas that are addressable by a common bit line group exceeds a second maximum number of defective memory areas (Figure 2 # 216 & # 218, claim 29).

Beffa et al. does not explicitly teach an overflow register.

However, Bemis in an analogous art teaches a memory array with an overflow register that detects overflow (Abstract lines 3-10). It would have been obvious to one of

ordinary skill in the art at the time the invention was made to enable Beffa et al.'s invention to be able to detect overflow, because one of ordinary skill in the art would have realized that including an overflow register would have prevented data loss.

Claims 1, 7, 15 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsutsumi et al. US Pat no. 6,115,828 and further in view of Eaton et al. US Pat no. 4,939,694.

As per claims 1, 7, 15 and 18:

Tsutsumi et al. substantially teaches a method, test device, test system and method for determining for determining a repair solution for a memory module in a test system, comprising: determining, for each memory area of the memory module a defect datum (Figure 11 # 15); generating defect addresses for all defective memory areas (Figure 11 # 41 & 46); storing the defect addresses in the test system (Figure 11); and selecting one or more replacement redundant groups based on the defect addresses stored in the test system (Figure 11 # 32), wherein each memory area is addressable via a word line group comprising one or more word lines or via a bit line group comprising one or more bit lines (claims 1-3).

Tsutsumi et al. does not explicitly teach a method, test device, test system and method for determining for determining a repair solution for a memory module in a test system, wherein the one or more replacement redundant groups are selected from a redundant word line group if the defective memory areas that are addressable by a common word line group exceeds a first maximum number and from a redundant bit line

group if the defective memory areas that are addressable by a common bit line group exceeds a second maximum number.

However Eaton et al. in an analogous art teaches the method wherein the one or more replacement redundant groups are selected from a redundant word line group if the defective memory area exceeds a maximum number (columns 5-6, lines 60-15). It would have been obvious to one of ordinary skill in the art at the time the invention was made to enable Tsutsumi's invention with error correction and replacement capabilities of Eaton, because one of ordinary skill in the art would have realized that doing so will enable Tsutsumi's invention to perform memory testing more efficiently. For instance after detection or error in a bit line or a word line the apparatus in Tsutsumi will determine how many errors are in one group, if there are only a few errors then using Eaton's techniques the apparatus in Tsutsumi will correct the defective memory cells as opposed to substituting the whole bit line or word line. However, if the number of defective memory cells exceeds a first or second maximum number, where error correction will not be an efficient option then in that case it will be advantageous to substitute the entire word or bit group, making the testing procedure more efficient.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Examiner's Note: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant, in preparing the responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Saqib Siddiqui
Art Unit 2138
05/17/2007

/Cynthia Britt/
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